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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/395,294	09/13/1999	SOPHIE WILSON	1073/OG117	5796

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EXAMINER
DECKTER, STEPHANIE M

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 01/15/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

H-G

Office Action Summary	Application No.	Applicant(s)	
	09/395,294	WILSON, SOPHIE	
	Examiner	Art Unit	
	Stephanie M. Deckter	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09/13/99, 06/09/00, and 06/26/00* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Papers Submitted

1. It is hereby acknowledged that the following papers have been received and placed of record in the file:

Formal Drawings as received on 06/09/00.

Information Disclosure Statement as received on 06/26/00.

Drawings

2. The formal drawings were received on 06/09/00. These drawings are acceptable to the examiner.

Specification

3. The disclosure is objected to because of the following informalities:

Applicant attempts to incorporate a copending application by reference on the 10th line of the second paragraph on the 6th page of the specification. However, applicant neglects to list the serial number and title of such copending application.

On the 11th line of the second paragraph of the 9th page of the specification, please change "format (3)" to "format L3" to correctly reference figure 5.

Appropriate correction is required.

Claim Objections

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1 and 3 are objected to under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which

applicant regards as the invention. Claim 1 recites the limitation "control the first and second channels in dependence on said detection" in the 11th and 12th line of the claim. This language is unclear and it appears applicant meant to state "control the first and second channels independently upon said detection." Appropriate correction is required.

Claim 3 recites the limitation "controls the first and second channels each to simultaneously execute the single operation" in the 2nd & 3rd lines of the claim. This limitation is can mean both channels simultaneously execute the same exact operation, i.e. using the same data, **or** each channel simultaneously executes the operation using separate data, i.e. the channels cooperate to perform the operation. In view of the specification, and limitations set forth in claim 8, it appears that applicant intended on the latter meaning. Examiner suggests the following change to claim 3 for clarification of this issue: "controls the first and second channels each to simultaneously execute the single operation on different data."

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C.

122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

7. Claims 12-13 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Fleck et al., U.S. Patent Number 6,292,845. Referring to claim 12, Fleck has taught a computer program product comprising program code means which include

a. a sequence of instructions (column 2, lines 44-45 and 49-50, figure 1, element 1) all having the same predetermined bit length (column 2, lines 51-53 and figure 1, element 3),

b. said instructions including long instructions wherein said predetermined bit length defines a single operation (figure 2, element 219)

c. and dual operation instructions wherein said predetermined bit length defines two independent operations (figure 2, element 206),

d. wherein the computer program product is adapted to run on a computer such that the long instructions control the resources of the computer in a first way, and the dual operation instructions control the resources of the computer in a second way (column 3, lines 33-38).

8. Referring to claim 13, Fleck has taught a computer product wherein each instruction includes a set of identification bits at designated bit locations within the instruction (figure 3a), said identification bits being adapted to cooperate with a decode unit of a computer system (column 2, lines 52-55 and figure 1, element 7) to designate whether the instruction is a long instruction or a dual operation instruction (column 4, line 63 to column 5, line 7).

9. Referring to claim 16, Fleck has taught a computer program product comprising program code means which include

a. a sequence of instructions (column 2, lines 44-45 and 49-50, figure 1, element 1) all having the same predetermined bit length (column 2, lines 51-53 and figure 1, element 3),

b. said instructions including long instructions wherein said predetermined bit length defines a single operation (figure 2, element 219)

c. and dual operation instructions wherein said predetermined bit length defines two independent operations (figure 2, element 206),

d. said instructions including a set of identification bits at designated bit locations within the instruction (column 4, line 63 to column 5, line 7 and figure 3a)

e. wherein the computer program product is adapted to run on a computer such that said identification bits are adapted to cooperate with a decode unit of the computer (column 2, lines 52-55 and figure 1, element 7) to designated whether:

i. the instruction is a long instruction or a dual operation instruction (column 4, line 67 to column 5, line 3 and figure 3a, Bit 0); and

ii. in the case of dual operation instruction, the nature of each operation in the instruction selected from a data processing category and a memory access category (column 5, lines 3-7, column 2, lines 12-13 and 18-20 and figure 3a, Bit 1).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1, 2, 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fleck et al., U.S. Patent Number 6,292,845 (herein referred to as Fleck) in view of Shiell et al., U.S. Patent Number 6,317,820 (herein referred to as Shiell). Referring to claim 1, Fleck has taught a computer system comprising

a. a decode unit for decoding instructions (column 2, lines 52-55 and figure 1, element 7) fetched from a memory holding a sequence of instructions (column 2, lines 44-45 and 49-50, figure 1, element 1), all instructions in the sequence having the same predetermined bit length (column 2, lines 51-53 and figure 1, element 3); and

b. first and second processing channels (column 2, lines 4-5 and figure 1, elements 10 and 11)

c. wherein the decode unit is operable to detect for each instruction of said predetermined bit length whether the instruction defines a single operation or two independent operations (column 4, line 67 to column 5, line 3, figure 1, element 7 and figure 3a) and to control the first and second channels in dependence on said detection (column 2, lines 55-65).

Fleck has not taught the first and second processing channels where each channel comprises a plurality of functional units, at least one of said functional units in each channel being a data processing unit and at least one other of said functional units in each channel being a memory access unit. Shiell has taught first and second processing channels, each channel comprising a plurality of functional units, at least one of said functional units in each channel being a data processing unit and at least one other of said functional units in each channel being a memory

access unit (Shiell column 3, lines 54-61 and figure 1, elements 130A and 130B which include elements S1, L1, M1, D1, S2, L2, M2, and D2). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to replace the first and second processing channels of Shiell with the processing channels of Fleck having data processing and memory access units in each channel. Doing so would have been beneficial in that task-level parallelism would have been increased due to the greater number of functional units of the processor (Shiell column 1, lines 16-39).

12. Referring to claim 2, Fleck has taught when the decode unit detects that the instruction defines two independent operations, it is operable to control the first channel to implement one of those operations and the second channel to implement the other of those operations, whereby the first and second channels execute their respective independent operations simultaneously (column 3, lines 33-39).

13. Referring to claim 5, Fleck has taught the decode unit operable to make said detection based on the values of a designated set of identification bits at predetermined bit locations in the instruction (figure 1, element 7 and column 4, line 63 to column 5, line 7 and figure 3a).

14. Referring to claim 6, Fleck and Shiell have taught each limitation of claim 6, including an instruction having a length of n bits wherein one of the predetermined bit locations include the nth and (n+1)st bit. The other predetermined bit location including the n/2th bit has not been taught. However, changing the predetermined location of the second identification bit from the (n+1)st bit to the n/2th bit would have been an obvious improvement. One of ordinary skill in the art would have been motivated to do so in order to better tag or track information regarding

the second operation of the instruction by moving the bit closer to such instruction. Also see In re Japikse, **86 USPQ 70 (CCPA 1950)**.

15. Referring to claim 7, Fleck has taught a decode unit operable to identify certain combinations of said independent operations in an instruction based on said set of identification bits, wherein a first combination denotes two data processing operations, a second combination denotes two memory access operations, a third combination denotes a data processing operation and a memory access operation and a fourth combination denotes a long instruction (column 3, lines 15-24, 33-52, figure 2, column 4, line 63 to column 5, line 7 and figure 3A).

16. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fleck et al., U.S. Patent Number 6,292,845 in view of Shiell et al., U.S. Patent Number 6,317,820 and further in view of Mohamed, U.S. Patent Number 6,230,180. Fleck and Shiell have taught each limitation of claim 3, including detection by the decode unit that an instruction defines a single operation (column 4, line 67 to column 5, line 3, figure 1, element 7 and figure 3a) as well as control of the first and second processing channels by the decode unit (column 2, lines 55-65). The further limitation that the first and second channels each simultaneously execute the single operation has not been taught. Mohamed has taught simultaneous execution of a single instruction with multiple data (column 1, lines 59-64). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to utilize the method of simultaneous execution of a single instruction with multiple data within the functional units of the first and second processing channels of Shiell. Doing so would have been beneficial in order to increase data parallelism (Mohamed column 1, lines 64-67) by reducing the size of necessary program memory in that

only one copy of the code being simultaneously executed is required, as opposed to a copy for each functional unit.

17. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fleck et al., U.S. Patent Number 6,292,845 in view of Shiell et al., U.S. Patent Number 6,317,820 and further in view of Mukhanov, U.S. Patent Number 5,365,476. Shiell and Fleck have taught each limitation of claim 4, including first and second channels sharing at least one common register file (column 4, lines 24-29 and figure 1, elements 140A and 140B). However, simultaneous access of the register file by the channels has not been explicitly taught. Mukhanov has taught a register file that can be simultaneously accessed by more than one functional unit (Mukhanov column 2, lines 34-43). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to utilize the register file of Mukhanov as the register file of Shiell. Doing so would have been beneficial in that a dual read port would save cycles otherwise required for register fetch operations if the register file could only be accessed by one functional unit at a time (Mukhanov column 2, lines 44-47).

18. Claims 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fleck et al., U.S. Patent Number 6,292,845 in view of Shiell et al., U.S. Patent Number 6,317,820 and further in view of Mohamed, U.S. Patent Number 6,230,180. Referring to claim 8, Fleck has taught a method of operating a computer system which comprises

a. first and second processing channels (column 2, lines 4-5 and figure 1, elements 10 and 11), the method comprising

b. decoding an instruction (column 2, lines 52-55 and figure 1, element 7) having a predetermined bit length (column 2, lines 51-53 and figure 1, element 3) to detect whether that instruction defines a single operation or two independent operations (column 4, line 67 to column 5, line 3, figure 1, element 7 and figure 3a);

c. where the instruction defines two independent operations, supplying one of the operations to the first processing channel and the other of the operations to the second processing channel whereby the operations are executed simultaneously (column 3, lines 33-39).

d. when the instruction defines a single operation, controlling the first and second processing channels (column 2, lines 55-65).

Fleck has not taught the first and second processing channels where each channel comprises a plurality of functional units, at least one of said functional units in each channel being a data processing unit and at least one other of said functional units in each channel being a memory access unit. Shiell has taught first and second processing channels, each channel comprising a plurality of functional units, at least one of said functional units in each channel being a data processing unit and at least one other of said functional units in each channel being a memory access unit (Shiell column 3, lines 54-61 and figure 1, elements 130A and 130B which include elements S1, L1, M1, D1, S2, L2, M2, and D2). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to replace the first and second processing channels of Shiell with the processing channels of Fleck having data processing and memory access units in each channel. Doing so would have been beneficial in that task-level parallelism would have been increased due to the greater number of functional units of the

processor (Shiell column 1, lines 16-39). Furthermore, Fleck has not taught the further limitation that the first and second channels cooperate to execute the single operation. Mohamed has taught simultaneous execution of a single instruction with multiple data (column 1, lines 59-64), i.e. cooperation among functional units to execute a single operation. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to utilize the method of cooperative execution of a single instruction with multiple data within the functional units of the first and second processing channels of Shiell. Doing so would have been beneficial in order to increase data parallelism (Mohamed column 1, lines 64-67), i.e. a single operation can be executed faster if more than one functional unit operates on the associated data.

19. Referring to claim 9, Fleck has taught the step of decoding and detecting comprises reading the values of a designated set of identification bits at predetermined bit locations in the instruction (column 4, line 63 to column 5, line 7 and figure 3a).

20. Referring to claim 10, Fleck has taught said designated bits are used to denote the nature of independent operations when the instruction defines two operations (column 2, lines 14-15 and 18-20), in addition to designating that the instruction defines a single operation (column 4, line 63 to column 5, line 7 and figure 3a).

21. Referring to claim 11, Fleck has taught an instruction having a length of n bits wherein one of the predetermined bit locations includes the nth bit and the other predetermined bit location includes the (n+1)st bit. The other predetermined bit location including the n/2th bit has not been taught. However, changing the predetermined location of the second identification bit from the (n+1)st bit to the n/2th bit would have been an obvious improvement. One of ordinary skill in the art would have been motivated to do so in order to better tag or track information

regarding the second operation of the instruction by moving the bit closer to such instruction. Also see In re Japikse, **86 USPQ 70 (CCPA 1950)**.

22. Claims 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fleck et al., U.S. Patent Number 6,292,845. Fleck has taught each limitation of claim 14, including an instruction having a length of n bits wherein one of the predetermined bit locations includes the nth bit and the other predetermined bit location includes the (n+1)st bit. The other predetermined bit location including the n/2th bit has not been taught. However, changing the predetermined location of the second identification bit from the (n+1)st bit to the n/2th bit would have been an obvious improvement. One of ordinary skill in the art would have been motivated to do so in order to better tag or track information regarding the second operation of the instruction by moving the bit closer to such instruction. Also see In re Japikse, **86 USPQ 70 (CCPA 1950)**.

23. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fleck et al., U.S. Patent Number 6,292,845 in view of Shiell et al., U.S. Patent Number 6,317,820. Fleck has taught a method of operating a computer system which comprises

a. first and second processing channels (column 2, lines 4-5 and figure 1, elements 10 and 11), the method comprising

b. fetching a sequence of instructions from a program memory (column 2, lines 44-45 and 49-50, figure 1, element 1), all said instructions having the same predetermined bit length (column 2, lines 51-53 and figure 1, element 3) and containing a set of designated

bits at predetermined bit locations within said bit length (column 4, line 63 to column 5, line 7 and figure 3a);

c. decoding each instruction (column 2, lines 52-55 and figure 1, element 7), said decoding step including reading the values of said designated bits to determine:

i. whether the instruction defines a single operation or two independent operations (column 4, line 67 to column 5, line 3 and figure 3a, Bit 0); and

ii. where the instruction defines two independent operations, the nature of each of those operations selected at least from a data processing category of operation and a memory access category of operation (column 5, lines 3-7, column 2, lines 12-13 and 18-20 and figure 3a, Bit 1).

Fleck has not taught the first and second processing channels where each channel comprises a plurality of functional units, at least one of said functional units in each channel being a data processing unit and at least one other of said functional units in each channel being a memory access unit. Shiell has taught first and second processing channels, each channel comprising a plurality of functional units, at least one of said functional units in each channel being a data processing unit and at least one other of said functional units in each channel being a memory access unit (Shiell column 3, lines 54-61 and figure 1, elements 130A and 130B which include elements S1, L1, M1, D1, S2, L2, M2, and D2). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to replace the first and second processing channels of Shiell with the processing channels of Fleck having data processing and memory access units in each channel. Doing so would have been beneficial in that task-level

parallelism would have been increased due to the greater number of functional units of the processor (Shiell column 1, lines 16-39).

Conclusion

24. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

Eickemeyer et al., U.S. Patent Number 5,355,460, have taught a system capable of processing two or more fixed length and tagged instructions in parallel on a plurality of functional units.

Krishnan et al., Japanese Patent Number JP2001142692A, have taught execution of 32-bit instructions comprising either two 16-bit fixed length operations or one 32-bit fixed length operation on a single machine.

Laurenti et al., Japanese Patent Number JP2000215061A, have taught decoders arranged to respond to a tag in a tag field in the instruction buffer which indicates whether the buffered instruction is a single or a compound instruction.

Van Eijndhoven et al., U.S. Patent Number 6,076,154, have taught first and second functional units for executing first and second commands within a first instruction word.

Yates, Jr. et al., U.S. Patent Number 5,051,885, have taught a bit field indicating the type and length of an instruction word comprising two operations.

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephanie M. Deckter whose telephone number is 703-308-6132. The examiner can normally be reached on 8:00 A.M. - 5:30 P.M. with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Stephanie M. Deckter SMD
Examiner
Art Unit 2183

December 20, 2001

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